# AND8256/D

# Control of the Output Voltage Range in NCP1653 Driven PFC Stages

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APPLICATION NOTE

*The NCP1653 embeds two functions to ease and optimize the design of your PFC stage:*

- *One of them is the so called "follower boost mode". When applied (it is optional), it makes the preconverter output voltage stabilize at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the difference between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage (refer to MC33260 and NCP1653 data sheet at www.onsemi.com).*
- *Also, instead of a traditional high gain integrator that tends to overreact tardily, the NCP1653 incorporates a low gain regulator to bring a more gradual response. Given that the low regulation bandwidth of PFC stages leads to a high inertia and poor dynamic performance (high output over and undershoots when the load abruptly changes), such a gain reduction improves the dynamic behavior and the stability at the price of a very limited variation of the regulation voltage (the output regulation voltage is slightly lowered when the AC line current demand is maximal − 96% of the regulation high level).*

*Finally, if these two functions (follower boost, low gain regulator) bring significant benefits, one must admit that they also tend to increase the output voltage spread and … the number of questions from designers who do not necessarily feel comfortable with these variations. These are the concerns this paper aims at clearing up.*

## INTRODUCTION

### NCP1653 Dimensioning

An Excel spreadsheet (based on the AND8184 application note, both being available at www.onsemi.com) automatically computes the external components necessary to build a PFC stage as portrayed by Figure 1.

One can summarize the following key steps:

- Select the feedback resistor to set the regulation level.
- Choose $R_{SENSE}$ and $R_{CS1}$ of Figure 1 to set the maximum coil current limit.
- Dimension $R_{IN1}$ and $R_{IN2}$ to set the right power limit in conjunction with the already selected $R_{SENSE}$ and $R_{CS1}$ resistances.
- Select $R_{CS2}$ to adjust the PFC output voltage range.

More specifically,

- If you select a "*high*" resistance for $R_{CS2}$, you set the follower boost mode: a large variation of the output voltage is allowed to optimize both the size and the cost of the PFC stage.
- If the downstream converter needs a narrow input voltage range for proper operation (like for instance, forward or half−bridge power supplies), the Follower Boost mode is to be avoided. In this case, $R_{CS2}$ must be selected "*low*" enough to cancel this mode.
- If you further lower the $R_{CS2}$ resistance, you tend to increase the regulation gain and hence, the output voltage accuracy. The gain of the regulation loop is nominally set relatively low to improve the dynamic behavior of the PFC stage at the price of a typically 4% variation of the regulation voltage (the output regulation voltage is slightly reduced when the AC line current demand is maximum 96% of the regulation high level).

The goal of this paper is to describe the meaning of the terms "*high*" and "*low*", and to explain what is behind the "*Follower boost mode*" and "*the regulation gain*".



February, 2006 − Rev. 0

Publication Order Number:
AND8256/D

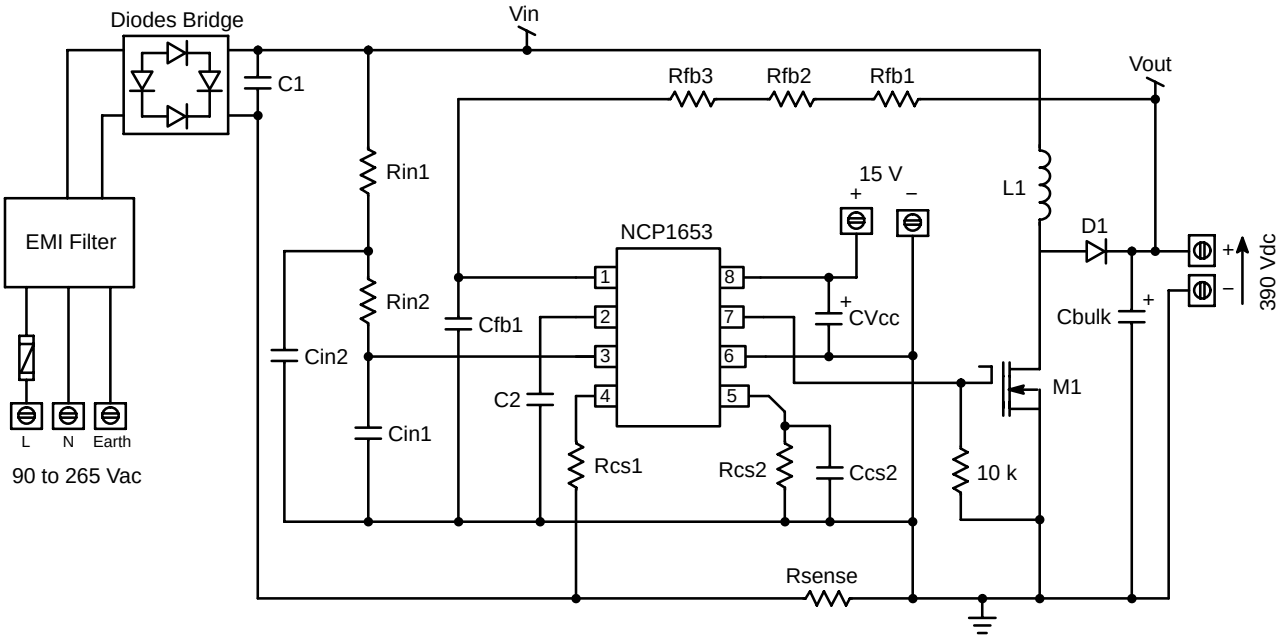


**Figure 1. Generic Schematic**

## THE SOURCE OF OUTPUT VOLTAGE VARIATIONS

## 1. Follower Boost Mode

Traditionally, a PFC stage is actually a boost pre−regulator that outputs a constant DC voltage (390 V typically). Now, if the downstream converter that loads the PFC stage can handle some variations of its input voltage, and if your hold−up time specification is not too severe, why not let the PFC stage output stabilize at a DC level that varies within a controlled range (for instance, between 200 and 400 V in a wide mains application)?

That is the idea behind the “Follower Boost” mode: the output voltage of the PFC stage stabilizes at a level that linearly varies versus the AC line amplitude. This technique aims at reducing the difference between the output and input voltages.

Such an option may appear strange until you note that the efficiency of boost converters increases when the difference between the output and input voltages is reduced.

Two equations highlight the benefits of this mode:

− The formula that expresses the MOSFET duty cycle: $d = 1-\frac{V_{IN}}{V_{OUT}}$ that clearly shows that the MOSFET duty cycle decreases when the output voltage is reduced. For instance, if the input voltage is 120 V, the duty cycle is 70% when $V_{OUT}$ = 400 V and 40% when $V_{OUT}$ is 200 V. In other words, the follower boost limits “d” and hence, the portion of the coil current that flows through the MOSFET. *Consequently, this operation mode drastically reduces the conduction losses.*

− The expression of the current ripple: $\frac{Vin}{L \cdot f} \cdot \left(1-\frac{Vin}{Vout}\right) = \frac{Vin}{L \cdot f} \cdot d$ shows that the coil current ripple is proportional to the duty cycle and hence, that the follower boost tends to decrease it. You immediately understand that the follower boost allows the use of a smaller inductor for the same specified ripple. Given that in practice, the coil inductance is chosen high enough to limit the AC component of the current to an acceptable level, *the Follower Boost mode lowers the size and the cost of your coil*. Figure 4 portrays this benefit in a 300 W, wide mains application.

In addition, it is clear that a reduction of the output voltage leads to a *diminution of the switching losses.* This is the third benefit of the technique.

### How Does It Work?

As shown in the data sheet, the following equation gives the maximum average power an NCP1653 driven PFC stage can provide the load with:

$$(P_{OUT})_{MAX} = \frac{K \cdot V_{AC}}{R_{CS2} \cdot V_{OUT}} \qquad \text{(eq. 1)}$$

Where:

$$K = \frac{\eta \cdot \pi \cdot R_{CS1} \cdot R_{IN} \cdot I_{REF} \cdot V_{REF}}{2\sqrt{2} \cdot R_{SENSE}} \qquad \text{(eq. 2)}$$

And:

- $R_{SENSE}$ is the resistor that senses the coil current
- $R_{CS1}$ is the resistor connected to Pin 4 to set the current limit
- $R_{CS2}$ is the resistor connected to Pin 5
- $R_{IN}$ is the input voltage sensing global resistance ($R_{IN} = R_{IN1} + R_{IN2}$)
- $I_{REF}$ is the internal current reference (200 μA)
- $V_{REF}$ is the internal voltage reference (2.5 V)
- $V_{AC}$ is the AC line rms voltage
- $V_{OUT}$ is the output voltage

($R_{SENSE}$, $R_{CS1}$, $R_{CS2}$, $R_{IN1}$ and $R_{IN2}$ are represented in Figure 1)

K and $R_{CS2}$ being constants, Equation 1 shows that at a given line magnitude, the power capability depends on the output voltage level. For instance, suppose that K and Rcs2 are dimensioned so that the low line power capability is 150 W if $V_{OUT}$ = 400 V, Equation 1 teaches us that the PFC stage will be able to provide 300 W only if $V_{OUT}$ drops to 200 V.

That is the follower boost principle: we dimension the NCP1653 external elements so that the PFC stage cannot provide the full power unless $V_{OUT}$ stabilizes at a target voltage that is low compared to the regulation level.

More specifically, one can deduct that the power capability (see Figure 2):

- Is inversely dependent of the output voltage and hence maximal at the lowest $V_{OUT}$ level ($V_{OUT} = V_{OUT,LL}$)
- Is proportional to the line magnitude and then, minimum at low line ($V_{AC} = V_{AC,LL}$)

Hence, one must compute Rcs2 so that the PFC stage can supply the full power at low line and at the minimum output voltage you want to set, and if $P_{MAX}$ is the targeted power capability:

$$R_{CS2} = \frac{K}{P_{MAX}} \cdot \frac{V_{AC,LL}}{V_{OUT,LL}} \qquad \text{(eq. 3)}$$

Combination of Equations 1 and 2 leads to:

- $V_{OUT} = V_{AC} \cdot \frac{P_{MAX}}{< P_{IN} >} \cdot \frac{V_{OUT,LL}}{V_{AC,LL}}$ , where <PIN> is the input power. This equation is valid as long as the output voltage is below the output regulation level ($V_{OUT,REG}$).
- $V_{OUT} = V_{OUT,REG}$, when the system tends to force $V_{OUT}$ to be higher than the regulation level (the regulation block clamps the follower boost characteristic).

This is the follower boost characteristic also portrayed by Figure 3.

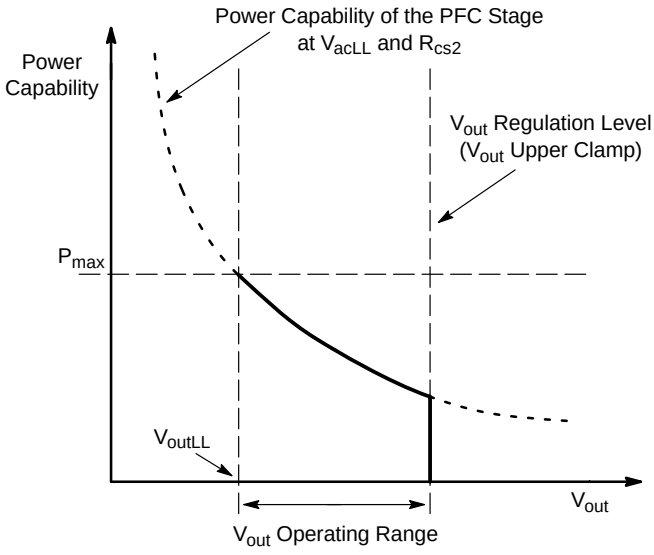


**Figure 2. Power capability of the PFC stage as a function of the output voltage level.**

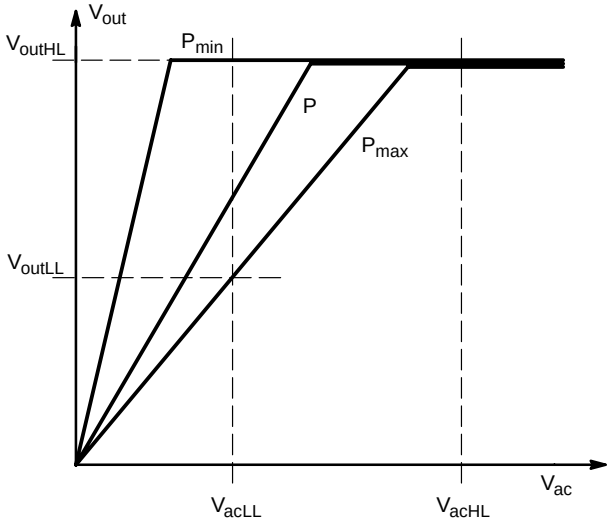


**Figure 3. Follower Boost Characteristic**

### Experimental Results

A performance comparison has been performed between the Follower Boost and traditional modes using the application of Figure 1 (300 W, wide mains). The measurements were made on the same boards. Simply the resistance of $R_{CS2}$ (R3 of Figure 1) was doubled and the coil inductance halved (as a benefit of this technique) for the tests in follower boost mode.

**Table 1. Performance Comparison between Follower Boost and Traditional Mode**

| Vac = 110 V | Follower Boost | | | Traditional Mode | | |
|---|---|---|---|---|---|---|
| Pin | Vout | Eff | THD | Vout | Eff | THD |
| (W) | (V) | (%) | (%) | (V) | (%) | (%) |
| 86 | 384 | 89 | 11 | 385 | 91 | 10 |
| 164 | 378 | 92 | 6.0 | 380 | 92 | 7.0 |
| 288 | 337 | 94 | 4.0 | 374 | 93 | 4.0 |
| 330 | 282 | 94 | 6.0 | 370 | 93 | 4.0 |

| Vac = 220 V | Follower Boost | | | Traditional Mode | | |
|---|---|---|---|---|---|---|
| Pin | Vout | Eff | THD | Vout | Eff | THD |
| (W) | (V) | (%) | (%) | (V) | (%) | (%) |
| 82 | 386 | 94 | 19 | 387 | 92 | 14 |
| 123 | 385 | 94 | 16 | 387 | 95 | 11 |
| 163 | 384 | 94 | 14 | 386 | 93 | 9.0 |
| 220 | 382 | 95 | 11 | 386 | 95 | 8.0 |
| 310 | 371 | 96 | 9.0 | 385 | 95 | 9.0 |

As shown by Table 1, the Follower Boost mode improves the efficiency without significantly degrading the THD. In addition, as shown by the following figure, the coil size is dramatically reduced. By the way, we can note that if needed, the coil could be made a bit less “squeezed’’ in order to minimize its losses and further improve the efficiency.

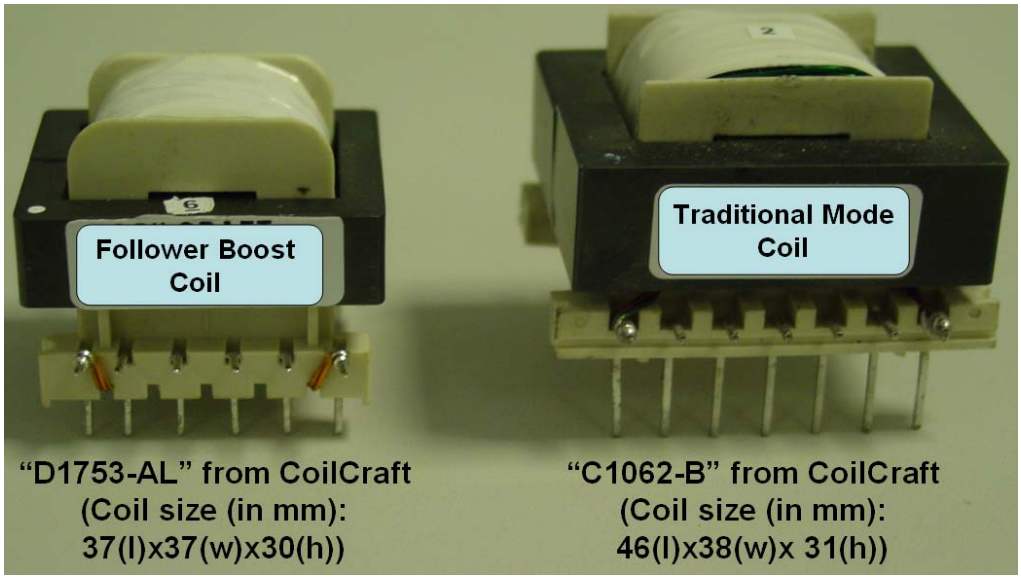


**Figure 4. CoilCraft Coils used for the Comparison**

**Is it Difficult to Implement?**

The design is straightforward:

- Download the NCP1653 design worksheet available at http://www.onsemi.com/pub/Collateral/NCP1653%20WORKSHEET..XLS .
- You want to operate in tradition mode: enter the regulation level you target (“Vout”) and enter the same value in the “VoutLL” cell like in Figure 5 and the Excel spreadsheet returns the maximum $R_{CS2}$ value you need to implement.
- You want to implement the follower boost: select the minimum output voltage you can accept in your application and fill “VoutLL” accordingly. For instance, enter 200 V like in Figure 6 and the Excel spreadsheet gives you the $R_{CS2}$ value to implement.

That’s it! In both cases, the Excel spreadsheet also computes the coil inductance and other key dimensioning elements.

| Please enter your specification | | | |
|---|---|---|---|
| fac | (Hz) | 60 | Ac line frequency |
| VacLL | (V) | 90 | Ac line rms lowest level (generally 85 V or 90 V in wide mains applications) |
| VacHL | (V) | 265 | Ac line rms highest level (generally 265 V in wide or European mains applications) |
| Vout | (V) | 390 | Wished regulation level for the output voltage (generally 390 V or 400 V in wide mains apps) |
| VoutLL | (V) | 390 | Minimum Output Voltage you can accept in normal operation - Use VoutLL=Vout as a default value if you don't know |
| eff | (%) | 92 | Expected efficiency at low line, full load - use 90 % as a default value if you don't know |
| Pout | (W) | 300 | Maximum output power |
| ΔIpk-pk | (%) | 30 | Targeted peak to peak ripple of the coil current at low line and full load - Use 30 % as a default value if you don't know |
| RdsON | (Ω) | 0.19 | MOSFET on-time resistance @ 25 °C |
| $T_{hold-up}$ | (ms) | 10 | Hold-up time. Put 0 if no hold-up time is specified or if you don't know. |
| (Vout)min | (V) | 300 | Minimum output Voltage you can accept at the end of the hold-up time - Don't fill this cell or put any value if no hold-up time is specified |
| %ΔVpk-pk | (%) | 7 | Peak to peak low frequency ripple that is acceptable across the bulk capacitor as a percentage of the regulation output voltage ("Vout"). |
| | | | Choose 7% if you don't know. |

**Figure 5. Excel Spreadsheet for Traditional Mode**

| Please enter your specification | | | |
|---|---|---|---|
| fac | (Hz) | 60 | Ac line frequency |
| VacLL | (V) | 90 | Ac line rms lowest level (generally 85 V or 90 V in wide mains applications) |
| VacHL | (V) | 265 | Ac line rms highest level (generally 265 V in wide or European mains applications) |
| Vout | (V) | 390 | Wished regulation level for the output voltage (generally 390 V or 400 V in wide mains apps) |
| VoutLL | (V) | 200 | Minimum Output Voltage you can accept in normal operation - Use VoutLL=Vout as a default value if you don't know |
| eff | (%) | 92 | Expected efficiency at low line, full load - use 90 % as a default value if you don't know |
| Pout | (W) | 300 | Maximum output power |
| ΔIpk-pk | (%) | 30 | Targeted peak to peak ripple of the coil current at low line and full load - Use 30 % as a default value if you don't know |
| RdsON | (Ω) | 0.19 | MOSFET on-time resistance @ 25 °C |
| $T_{hold-up}$ | (ms) | 10 | Hold-up time. Put 0 if no hold-up time is specified or if you don't know. |
| (Vout)min | (V) | 180 | Minimum output Voltage you can accept at the end of the hold-up time - Don't fill this cell or put any value if no hold-up time is specified |
| %ΔVpk-pk | (%) | 7 | Peak to peak low frequency ripple that is acceptable across the bulk capacitor as a percentage of the regulation output voltage ("Vout"). |
| | | | Choose 7% if you don't know. |

**Figure 6. Excel Spreadsheet for Follower Boost Mode**

## 2. Low Gain Regulator

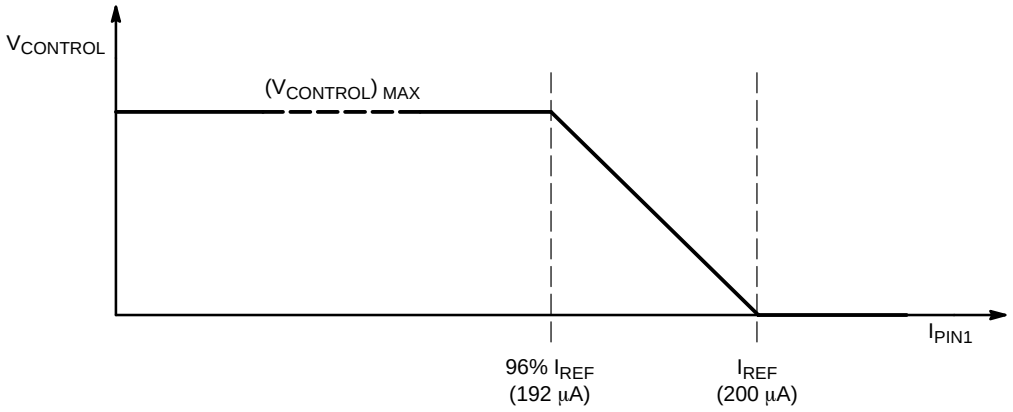


**Figure 7. Characteristic of the Low Gain Regulator**

The NCP1653 is designed to receive a current ($I_{pin1}$) that is proportional to the output voltage. $I_{pin1}$ is compared to the internal reference ($I_{REF}$ = 200 μA) following the characteristic of Figure 7. There are three cases:

- $I_{pin1}$ > 200 μA: the output of the regulation block is zero and the PFC stage provides no power
- $I_{pin1}$ < 96%.$I_{REF}$: the output of the regulation block is maximal $(V_{CONTROL})_{MAX}$). The PFC stage operates at its maximum power capability ($P_{MAX}$)
- 96%.$I_{REF}$ < $I_{pin1}$ < $I_{REF}$: the power that is delivered is adjusted as follows:

$$P = P_{MAX} \cdot \frac{I_{REF} - I_{pin1}}{I_{REF} - 96\% I_{REF}} = P_{MAX} \cdot \frac{I_{REF} - I_{pin1}}{4\% I_{REF}} \quad \text{(eq. 4)}$$

Hence, in nominal operation, the feedback current ($I_{pin1}$) must stabilize between (96%.$I_{REF}$) and $I_{REF}$, at the level that corresponds to the power demand:

$$I_{pin1} = I_{REF}\left[1 - \left(4\% \cdot \frac{P_{OUT}}{\eta \cdot P_{MAX}}\right)\right] \quad \text{(eq. 5)}$$

The Pin 1 current and the output voltage are proportional ($I_{pin1} = V_{OUT}/R_{OUT}$), where $R_{OUT}$ is the feedback resistor connected between the output voltage rail and Pin 1. Hence:

$$V_{OUT} = R_{OUT} \cdot I_{REF}\left[1 - \left(4\% \cdot \frac{P_{OUT}}{\eta \cdot P_{MAX}}\right)\right] \quad \text{(eq. 6)}$$

**What is $P_{MAX}$?**

$P_{MAX}$ is the maximum power the PFC stage can deliver. This power level is obtained when $V_{CONTROL}$ is maximum ($V_{CONTROL}$=$(V_{CONTROL})_{MAX}$) and one can show that it depends on the line magnitude and on some external components as follows:

$$P_{MAX} = \frac{\pi \cdot R_{CS1} \cdot R_{IN} \cdot V_{REF} \cdot I_{REF}}{2\sqrt{2} \cdot R_{CS2} \cdot R_{SENSE} \cdot V_{OUT}} \cdot V_{AC} \quad \text{(eq. 7)}$$

where:

- $R_{SENSE}$ is the resistor that senses the coil current
- $R_{CS1}$ is the resistor connected to Pin 4 to set the current limit
- $R_{CS2}$ is the resistor connected to Pin 5
- $R_{IN}$ is the input voltage sensing global resistance ($R_{IN} = R_{IN1} + R_{IN2}$)
- $I_{REF}$ is the internal current reference (200 μA)
- $V_{REF}$ is the internal voltage reference (2.5 V)
- $V_{AC}$ is the AC line rms voltage
- $V_{OUT}$ is the output voltage

($R_{SENSE}$, $R_{CS1}$, $R_{CS2}$, $R_{IN1}$ and $R_{IN2}$ are represented in Figure 1)

Provided that:

- $I_{REF}$ and $V_{REF}$ are constant values (200 μA and 2.5 V respectively)
- The application directly dictates the value of $R_{SENSE}$, $R_{CS1}$ and $R_{IN}$:
  - $R_{SENSE}$ and $R_{CS1}$ are designed to set the current limit so that: $R_{SENSE} \cdot I_{MAX} = R_{CS1} \cdot I_{REF}$, where $I_{MAX}$ is the maximum coil current.
  - $R_{IN}$ sets the power limit in conjunction with the chosen $R_{SENSE}$ and $R_{CS1}$ resistors as follows:

$$R_{IN} \cong \frac{\left(2 * \sqrt{2} * V_{AC,LL} I\pi\right)}{15\ \mu A}$$

Finally, $P_{MAX}$ only depends on $R_{CS2}$, $V_{OUT}$ and $V_{AC}$.

At a given $R_{CS2}$, if one considers $V_{OUT}$ as a constant (no follower boost), the power capability is only an increasing function of the line rms magnitude ($V_{AC}$), $P_{MAX}(V_{AC})$, that is minimum at the lowest rms level of the line ($V_{AC,LL}$):

$$P_{MAX}(V_{ACLL}) = \frac{\pi \cdot R_{CS1} \cdot R_{IN} \cdot V_{REF} \cdot I_{REF}}{2\sqrt{2} \cdot R_{CS2} \cdot R_{SENSE} \cdot V_{OUT}} \cdot V_{AC} \quad \text{(eq. 8)}$$

And:

$$P_{MAX} = P_{MAX}(V_{AC}) = \frac{V_{AC}}{V_{AC,LL}} \cdot P_{MAX}(V_{AC,LL}) \quad \text{(eq. 9)}$$

Finally, substitution of Equation 9 into Equation 6 leads to:

$$V_{OUT} = R_{OUT} \cdot I_{REF} \cdot \left(1 - \left(4\% \cdot \frac{V_{AC,LL}}{V_{AC}} \cdot \frac{P_{IN}}{P_{MAX}(V_{AC,LL})}\right)\right) \quad \text{(eq. 10)}$$

Hence, the $V_{OUT}$ absolute variation is:

$$\frac{\Delta V_{OUT}}{V_{OUT,REG}} = 4\% \cdot \frac{V_{AC,LL}}{V_{AC}} \cdot \frac{P_{IN}}{P_{MAX}(V_{AC,LL})} \quad \text{(eq. 11)}$$

Where:

$V_{OUT,REG}$ is the regulation level:

$$(V_{OUT,REG} = R_{OUT} \cdot I_{REF}) \quad \text{(eq. 12)}$$

This variation is then maximal at low line and full power:

$$\left(\frac{\Delta V_{OUT}}{V_{OUT,REG}}\right)_{MAX} = 4\% \cdot \frac{< P_{IN} >_{MAX}}{P_{MAX}(V_{AC,LL})} \quad \text{(eq. 13)}$$

When no follower boost is mandatory, the Excel spreadsheet[(1)] returns $R_{CS2}$ that makes the PFC stage supply the maximum power at low line when ($V_{CONTROL}$) is maximum. In other words, the low line power capability is limited to what is necessary to properly feed the load.

In this case:

$$P_{MAX}(V_{AC,LL}) = < P_{IN} >_{MAX}, \quad \text{(eq. 14)}$$

What is obtained if:

$$R_{CS2} = (R_{CS2})_T = \frac{\pi \cdot R_{CS1} \cdot R_{IN} \cdot V_{REF} \cdot I_{REF}}{2\sqrt{2} \cdot < P_{IN} >_{MAX} \cdot R_{SENSE} \cdot V_{OUT}} \cdot V_{AC,LL} \quad \text{(eq. 15)}$$

[1] $(R_{CS2})_T$ is the value that the Excel spreadsheet (available on the web to help dimension the PFC stage − refer to reference [3]) automatically returns if the value entered in the "VoutLL" cell equates that of the "Vout" one (see Table 1 and Figure 4).

Finally:

- If one chooses $R_{CS2} = (R_{CS2})_T$, the output voltage variation is 4%. In other words, the output voltage varies between 96% and 100% of the regulation level ($V_{OUT,REG} = R_{OUT} \bullet I_{REF}$). That means that if for instance, you set 390 V as the regulation level, $V_{OUT}$ will stabilize between 374 V and 390 V according to the line magnitude and the load.
- If $R_{CS2}$ is chosen lower than $(R_{CS2})_T$, $R_{CS2} = \alpha \cdot (R_{CS2})_T$, where $\alpha$ is a constant lower than 1:
  - $P_{MAX}(V_{AC,LL})$ is increased
  - And hence, the $V_{OUT}$ variation is reduced as follows:

$$\left(\frac{\Delta V_{OUT}}{V_{OUT,REG}}\right)_{MAX} = \alpha \cdot 4\% \cdot \frac{< P_{IN} >_{MAX}}{P_{MAX}(V_{AC,LL})} \quad \text{(eq. 16)}$$

For instance, if $R_{CS2}$ is halved, the spread is also halved.

As shown in the precedent section, if $R_{CS2} > (R_{CS2})_T$ the system enters the follower boost.

### Experimental Results

Some validation tests have been made on a 300 W demo board. They confirm the here above analysis.

The output regulation was measured over the line range (from 90 to 260 V) and at three different load currents (0.11 A, 0.40 A and 0.70 A that corresponds to the full load):

- First with $R_{CS2}$ = 48 kΩ that is roughly the value that theoretically leads to a variation between 96 and 100% of the regulation. In this case, the following figure shows that:
  - At low load, the output voltage keeps very closed to the regulation level (390 V) over the regulation.
  - The output voltage drops at low line and full power down to 376.5 V.
  - Finally the output voltage varies between 96.5% and 100% of the regulation voltage, which is in line with the expectation.

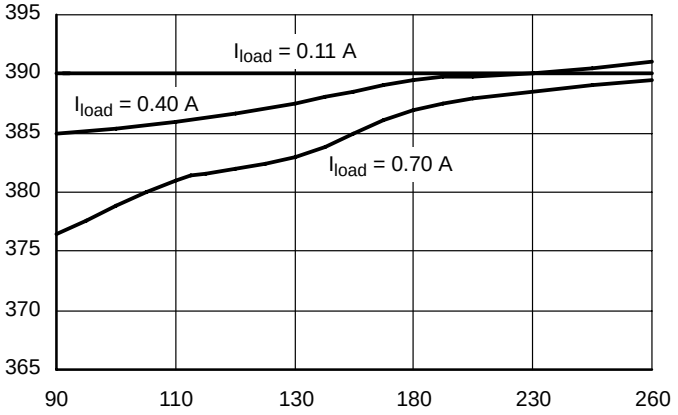


**Figure 8. Output Voltage versus Line and Load, with $R_{CS2}$ = 48 kΩ**

- Second with $R_{CS2}$ = 24 kΩ to see its effect on the output voltage accuracy and more specifically check if this division by two of $R_{CS2}$ halves the regulation spread. The following figure reports the results:

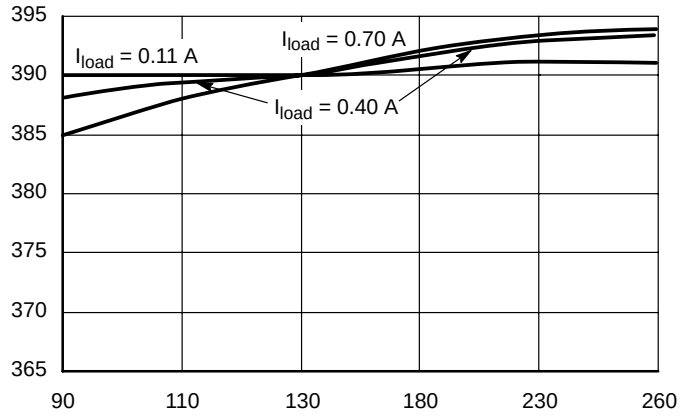


**Figure 9. Output Voltage versus Line and Load, with $R_{CS2}$ = 24 kΩ**

In this second case, one can note that:

- At low load, the output voltage still keeps very closed to the regulation level (390 V) over the regulation.
- As previously, the output voltage is minimal at low line and full power but that this level is much closer to the regulation level (385 V).
- Finally the output voltage varies between 98.7% and 100.7% of the regulation level, which is in line with the expectation.

Finally, one observes a good matching between the expectation and the experimental results [(2)].

## CONCLUSION

Once, you have dimensioned:

- The feedback resistor to set the regulation level
- The current sense resistors ($R_{SENSE}$, $R_{CS1}$) to set the maximum current limit
- The feedforward resistor ($R_{IN}$) to set the power limit

You finally have to define the Pin 5 resistor ($R_{CS2}$) to adjust the PFC stage power capability.

There is one key equation to select ($R_{CS2}$).

$$(R_{CS2})_T = \frac{\pi \cdot R_{CS1} \cdot R_{IN} \cdot V_{REF} \cdot I_{REF}}{2\sqrt{2} \cdot R_{SENSE} \cdot V_{OUT} \cdot < P_{IN} >_{MAX}} \cdot V_{AC,LL} \quad \text{(eq. 17)}$$

This equation gives the $(R_{CS2})_T$ value with respect to which ($R_{CS2}$) should be chosen, as follows:

- ($R_{CS2}$=$(R_{CS2})_T$): The PFC stage cannot provide more but the full power under the wished $V_{OUT}$. The output voltage is regulated between 96% and 100% of the regulation level.
- ($R_{CS2}$>$(R_{CS2})_T$): The PFC stage cannot supply the full power unless the output voltage decreases. You obtain a “Follower Boost” operation.
- ($R_{CS2}$<$(R_{CS2})_T$): This option increases the regulation gain and hence, the output voltage accuracy. The output voltage spread is divided by the [$(R_{CS2})_T$/$R_{CS2}$] ratio. For instance, if the ratio is 2, the output voltage will vary between 98% and 100% of the regulation level (2% variation instead of 4%).

The Overcurrent and Overpower limitations are not affected by the $R_{CS2}$ choice.

## References

1. NCP1653 data sheet and application notes available at www.onsemi.com.
2. “Further Optimize your Power Factor Correction Stage by Implementing the NCP1653 Follower Boost Mode’’ by Joel Turchi, “Power System Design’’ Magazine, August 2005 issue.
3. “NCP1653 PFC Boost Design Worksheet”, Excel based design aid that is available at http://www.onsemi.com/pub/Collateral/NCP1653%20WORKSHEET..XLS.

[2] Two second order effects were not taken into account in the study:
− The PFC stage efficiency: we generally consider the variation over the output power range while the output voltage actually depends on the input power.
− The output voltage ripple that is seen by the low gain regulator.
Practically they play a minor role.

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